In the Specification

At p. 1, please amend the "Related Patent Data" section as follows:

RELATED PATENT DATA

This patent resulted from a continuation application of U.S. Patent Application Serial No. 10/271,888, which was filed October 15, 2002 and which is a divisional of U.S. Patent Application Serial No. 09/592,604, which was filed June 12, 2000, and which issued on October 21, 2003 as U.S. Patent No. 6,635,552.

Please amend the paragraph starting at line 14 of page 18 as follows:

Referring to Fig. 13, a patterned masking layer is formed over some of base 102, while leaving ~~transistors gate~~ transistor gates 240 and 242, and regions proximate transistor gates 240 and 242, exposed. Insulative material sidewall spacers 272 are shown formed along sidewalls of transistor gate 242, and not along sidewalls of gate 240. Sidewall spacers 272 can be formed by conventional methods, including, by depositing and subsequently anisotropically etching an insulative material. [[the]] The spacers can be selectively formed to be only along sidewalls of gate 242, and not along sidewalls of gate 240, by, for example, initially forming spacers along sidewalls of both of gates 240 and 242, and subsequently protecting the spacers along gate 242 while etching the spacers from along gate 240. Sidewall spacers 272 can comprise, for example, silicon dioxide or silicon nitride. In typical processing, a protective mask would be formed over transistor gate 240 while sidewall spacers 272 are formed alongside transistor gate 242. Alternatively, spacers

could be formed alongside sidewalls of gate 240, as well as alongside the sidewalls of gate 242.